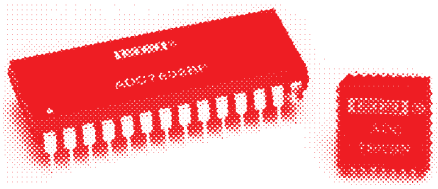
BURR - BROWN®



ADC7802

Autocalibrating, 4-Channel, 12-Bit ANALOG-TO-DIGITAL CONVERTER

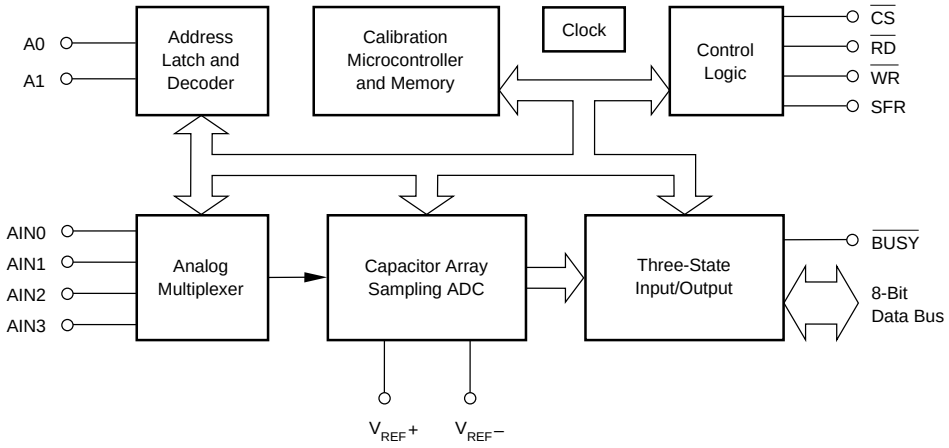
FEATURES

- **TOTAL UNADJUSTED ERROR ≤ 1/2LSB OVER FULL TEMPERATURE RANGE**
- **FOUR-CHANNEL INPUT MULTIPLEXER**
- **LOW POWER: 10mW plus Power Down Mode**
- **SINGLE SUPPLY: +5V**
- **FAST CONVERSION TIME: 8.5µs Including Acquisition**
- **AUTOCAL: No Offset or Gain Adjust Required**
- **UNIPOLAR INPUTS: 0V to 5V**
- **MICROPROCESSOR-COMPATIBLE INTERFACE**
- **INTERNAL SAMPLE/HOLD**

DESCRIPTION

The ADC7802 is a monolithic CMOS 12-bit A/D converter with internal sample/hold and four-channel multiplexer. An autocalibration cycle, occurring automatically at power on, guarantees a total unadjusted error within ±1/2LSB over the specified temperature range, eliminating the need for offset or gain adjustment. The 5V single-supply requirements and standard $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ control signals make the part very easy to use in microprocessor applications. Conversion results are available in two bytes through an 8-bit three-state output bus.

The ADC7802 is available in a 28-pin plastic DIP and 28-lead PLCC, fully specified for operation over the industrial –40°C to +85°C temperature range.



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Printed in U.S.A. June, 1993

SPECIFICATIONS

ELECTRICAL

At $V_A = V_D = V_{REF}+ = 5V \pm 5\%$; $V_A \geq V_D \geq V_{REF}+$; $V_{REF}-$ = AGND = DGND = 0V; CLK = 2MHz external with 50% duty cycle, T_A = –40°C to +85°C, after calibration cycle at any temperature, unless otherwise specified.

PARAMETER	CONDITIONS	ADC7802BP, ADC7802BN MIN	TYP	MAX	UNITS
RESOLUTION				12	Bits
ANALOG INPUT					
Voltage Input Range	$V_{REF}+$ = 5V, $V_{REF}-$ = 0V	0		5	V
Input Capacitance			50		pF
On State Bias Current			100		nA
Off State Bias Current	T_A = 25°C			10	nA
	T_A = –40°C to +85°C			100	nA
On Resistance Multiplexer			2		kΩ
Off Resistance Multiplexer			10		MΩ
Channel Separation	500Hz		92		dB
REFERENCE INPUT					
For Specified Performance: $V_{REF}+$	$V_{REF}+ \leq V_A$		5		V
$V_{REF}-$			0		V
For Derated Performance: [1] $V_{REF}+$		4.5		V_A	V
$V_{REF}-$		0		1	V
Input Reference Current	$V_{REF}+$ = 5V, $V_{REF}-$ = 0V		10	100	µA
THROUGHPUT TIMING					
Conversion Time With External Clock (Including	CLK = 2MHz, 50% Duty Cycle			8.5	µs
Multiplexer Settling Time and Acquisition Time)	CLK = 1MHz, 50% Duty Cycle			17	µs
	CLK = 500kHz, 50% Duty Cycle			34	µs
With Internal Clock Using	T_A = +25°C			10	µs
Recommended Clock Components	T_A = –40°C to +85°C		10		µs
Analog Signal Bandwidth [2]			500		Hz
Slew Rate [2]		8			mV/µs
Multiplexer Settling Time to 0.01%			460		ns
Multiplexer Access Time				20	ns
ACCURACY					
Total Adjusted Error,[3] All Channels				±1/2	LSB
Differential Nonlinearity				±1/2	LSB
No Missing Codes			Guaranteed		
Gain Error	All Channels			±1/4	LSB
Gain Error Drift	Between Calibration Cycles		±0.2		ppm/°C
Offset Error	All Channels			±1/4	LSB
Offset Error Drift	Between Calibration Cycles		±0.2		ppm/°C
Channel-to-Channel Mismatch				±1/4	LSB
Power Supply Sensitivity	$V_A = V_D$ = 4.75V to 5.25V		±1/8		LSB
DIGITAL INPUTS					
All Pins Other Than CLK: V_{IL}				0.8	V
V_{IH}		2.4			V
Input Current	T_A = +25°C, V_{IN} = 0 to V_D			1	µA
	T_A = –40°C to +85°C, V_{IN} = 0 to V_D			10	µA
CLK Input: V_{IL}				0.8	V
V_{IH}		3.5			V
I_{IL}				10	µA
I_{IH}				1.5	mA
I_{IH}	Power Down Mode (D3 in SFR HIGH)			100	nA
DIGITAL OUTPUTS					
V_{OL}	I_{SINK} = 1.6mA			0.4	V
V_{OH}	I_{SOURCE} = 200µA	4			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_D			±1	µA
Output Capacitance	High-Z State		4	15	pF
POWER SUPPLIES					
Supply Voltage for Specified Performance: V_A		4.75	5	5.25	V
V_D	$V_A \geq V_D$	4.75	5	5.25	V
Supply Current: I_A			1	2.5	mA
I_D	Logic Input Pins HIGH or LOW		1	2	mA
Power Dissipation	$\overline{WR}$ = $\overline{RD}$ = $\overline{CS}$ = $\overline{BUSY}$ = HIGH		10		mW
Power Down Mode	See Table III, Page 9		50		µW
TEMPERATURE RANGE					
Specification		–40		+85	°C
Storage		–65		+150	°C

NOTES: (1) For ($V_{REF}+$) – ($V_{REF}-$) as low as 4.5V, the total error will typically not exceed ±1LSB. (2) Faster signals can be accurately converted by using an external sample/hold in front of the ADC7802. (3) After calibration cycle, without external adjustment. Includes gain (full scale) error, offset error, integral nonlinearity, differential nonlinearity, and drift.

ABSOLUTE MAXIMUM RATINGS

V_A to Analog Ground	6.5V
V_D to Digital Ground	6.5V
Pin V_A to Pin V_D	±0.3V
Analog Ground to Digital Ground	±1V
Control Inputs to Digital Ground	–0.3V to V_D + 0.3V
Analog Input Voltage to Analog Ground	–0.3V to V_D + 0.3V
Maximum Junction Temperature	150°C
Internal Power Dissipation	875mW
Lead Temperature (soldering, 10s)	+300°C
Thermal Resistance, θ_{JA}: Plastic DIP	75°C/W
PLCC	75°C/W

ORDERING INFORMATION

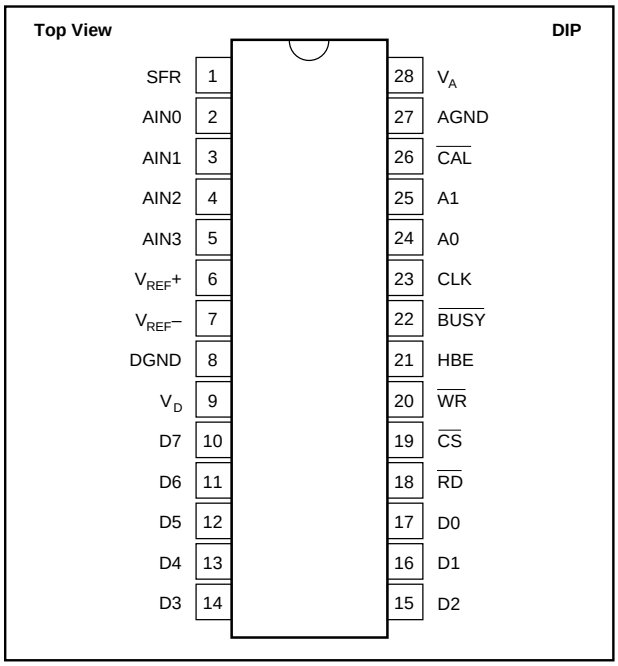
MODEL	MAXIMUM TOTAL ERROR, LSB	SPECIFICATION TEMPERATURE RANGE, °C	PACKAGE
ADC7802BN	±1/2	–40 to +85	PLCC
ADC7802BP	±1/2	–40 to +85	Plastic DIP

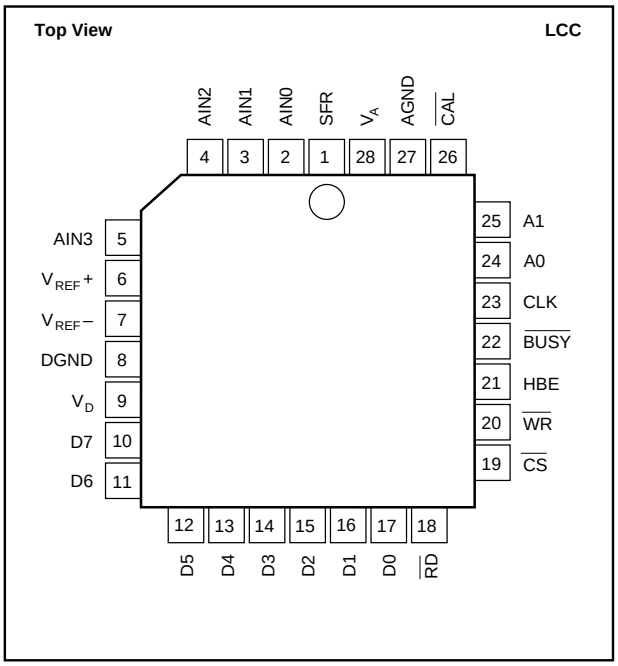
PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADC7802BN	28-Pin PLCC	251
ADC7802BP	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

PIN CONFIGURATIONS





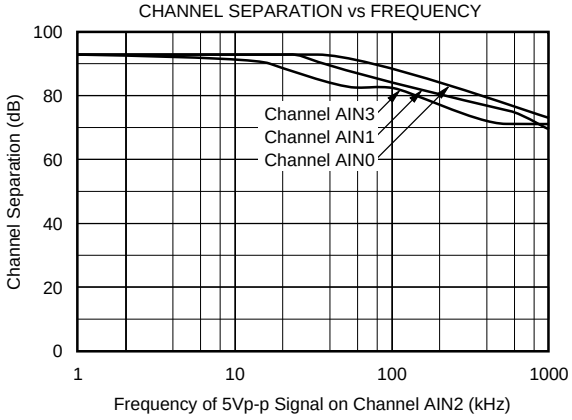
PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	SFR	Special Function Register. When connected to a microprocessor address pin, allows access to special functions through D0 to D7. See the sections discussing the Special Function Register. If not used, connect to DGND. This pin has an internal pull-down.
2 to 5	AIN0 to AIN3	Analog inputs. Channel 0 to channel 3.
6	V_{REF}+	Positive voltage reference input. Normally +5V. Must be ≤ V_A.
7	V_{REF}–	Negative voltage reference input. Normally 0V.
8	DGND	Digital ground. DGND = 0V.
9	V_D	Logic supply voltage. V_D = +5V. Must be ≤ V_A and applied after V_A.
10 to 17	D0 to D7	Data Bus Input/Output Pins. Normally used to read output data. See section on SFR (Special Function Register) for other uses. When SFR is LOW, these function as follows:
10	D7	Data Bit 7 if HBE is LOW; if HBE is HIGH, acts as converter status pin and is HIGH during conversion or calibration, goes LOW after the conversion is completed. (Acts as an inverted $\overline{BUSY}$.)
11	D6	Data Bit 6 if HBE is LOW; LOW if HBE is HIGH.
12	D5	Data Bit 5 if HBE is LOW; LOW if HBE is HIGH.
13	D4	Data Bit 4 if HBE is LOW; LOW if HBE is HIGH.
14	D3	Data Bit 3 if HBE is LOW; Data Bit 11 (MSB) if HBE is HIGH.
15	D2	Data Bit 2 if HBE is LOW; Data Bit 10 if HBE is HIGH.
16	D1	Data Bit 1 if HBE is LOW; Data Bit 9 if HBE is HIGH.
17	D0	Data Bit 0 (LSB) if HBE is LOW; Data Bit 8 if HBE is HIGH.
18	$\overline{RD}$	Read Input. Active LOW; used to read the data outputs in combination with $\overline{CS}$ and HBE.
19	$\overline{CS}$	Chip Select Input. Active LOW.
20	$\overline{WR}$	Write Input. Active LOW; used to start a new conversion and to select an analog channel via address inputs A0 and A1 in combination with $\overline{CS}$. The minimum $\overline{WR}$ pulse LOW width is 100ns.
21	HBE	High Byte Enable. Used to select high or low data output byte in combination with $\overline{CS}$ and $\overline{RD}$, or to select SFR.
22	$\overline{BUSY}$	$\overline{BUSY}$ is LOW during conversion or calibration. $\overline{BUSY}$ goes HIGH after the conversion is completed.
23	CLK	Clock Input. For internal/external clock operation. For external clock operation, connect pin 23 to a 74 HC-compatible clock source. For internal clock operation, connect pin 23 per the clock operation description.
24 to 25	A0 to A1	Address Inputs. Used to select one of four analog input channels in combination with $\overline{CS}$ and $\overline{WR}$. The address inputs are latched on the rising edge of $\overline{WR}$ or $\overline{CS}$. A1 / A0 / Selected Channel LOW / LOW / AIN0 LOW / HIGH / AIN1 HIGH / LOW / AIN2 HIGH / HIGH / AIN3
26	$\overline{CAL}$	Calibration Input. A calibration cycle is initiated when $\overline{CAL}$ is LOW. The minimum pulse width of $\overline{CAL}$ is 100ns. If not used, connect to V_D. In this case calibration is only initiated at power on, or with SFR. This pin has an internal pull-up.
27	AGND	Analog Ground. AGND = 0V.
28	V_A	Analog Supply. V_A = +5V. Must be ≥ V_D and V_{REF}+.

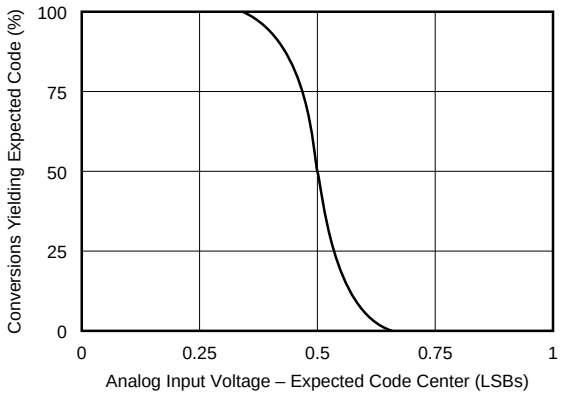
TYPICAL PERFORMANCE CURVES

At $V_A = V_D = V_{REF}+ = 5V$, $V_{REF}- = AGND = 0V$, $T_A = +25°C$, unless otherwise specified.

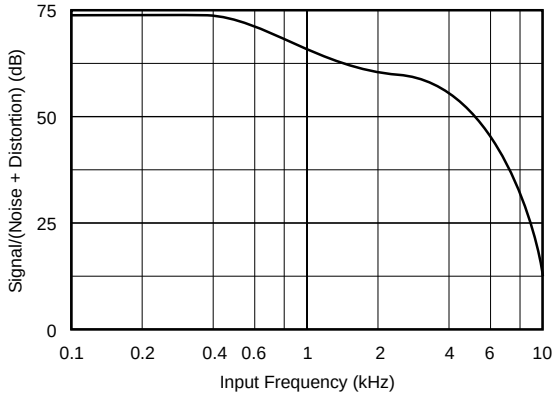
CHANNEL SEPARATION vs FREQUENCY



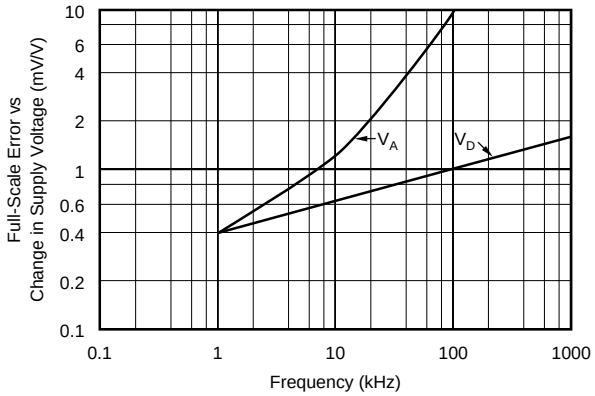
CODE TRANSITION NOISE



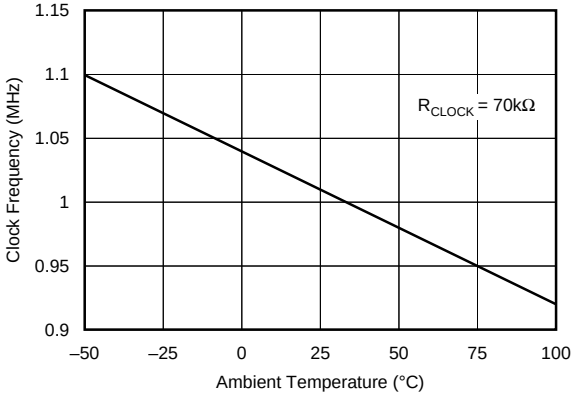
SIGNAL/(NOISE + DISTORTION)
vs INPUT FREQUENCY



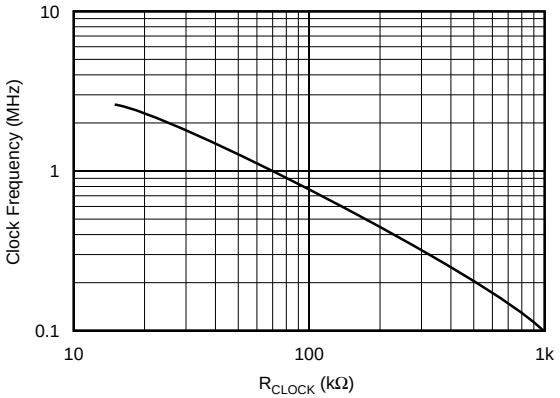
POWER SUPPLY REJECTION vs FREQUENCY



INTERNAL CLOCK FREQUENCY
vs TEMPERATURE



INTERNAL CLOCK FREQUENCY
vs R_{CLOCK}



THEORY OF OPERATION

ADC7802 uses the advantages of advanced CMOS technology (logic density, stable capacitors, precision analog switches, and low power consumption) to provide a precise 12-bit analog-to-digital converter with on-chip sampling and four-channel analog-input multiplexer.

The input stage consists of an analog multiplexer with an address latch to select from four input channels.

The converter stage consists of an advanced successive approximation architecture using charge redistribution on a capacitor network to digitize the input signal. A temperature-stabilized differential auto-zeroing circuit is used to minimize offset errors in the comparator. This allows offset errors to be corrected during the acquisition phase of each conversion cycle.

Linearity errors in the binary weighted main capacitor network are corrected using a capacitor trim network and correction factors stored in on-chip memory. The correction terms are calculated by a microcontroller during a calibration cycle, initiated either by power-up or by applying an external calibration signal at any time. During conversion, the correct trim capacitors are switched into the main capacitor array as needed to correct the conversion accuracy. This is faster than a complex digital error correction system, which could slow down the throughput rate. With all of the capacitors in both the main array and the trim array on the same chip, excellent stability is achieved, both over temperature and over time.

For flexibility, timing circuits include both an internal clock generator and an input for an external clock to synchronize with external systems. Standard control signals and three-state input/output registers simplify interfacing ADC7802 to most micro-controllers, microprocessors or digital storage systems.

Finally, this performance is matched with the low-power advantages of CMOS structures to allow a typical power consumption of 10mW.

OPERATION

BASIC OPERATION

Figure 1 shows the simple circuit required to operate ADC7802 in the Transparent Mode, converting a single input channel. A convert command on pin 20 ($\overline{WR}$) starts a conversion. Pin 22 ($\overline{BUSY}$) will output a LOW during the conversion process (including sample acquisition and conversion), and rises only after the conversion is completed. The two bytes of output data can then be read using pin 18 ($\overline{RD}$) and pin 21 (HBE).

STARTING A CONVERSION

A conversion is initiated on the rising edge of the $\overline{WR}$ input, with valid signals on A0, A1 and $\overline{CS}$. The selected input channel is sampled for five clock cycles, during which the comparator offset is also auto-zeroed to below 1/4LSB of error. The successive approximation conversion takes place during clock cycles 6 through 17.

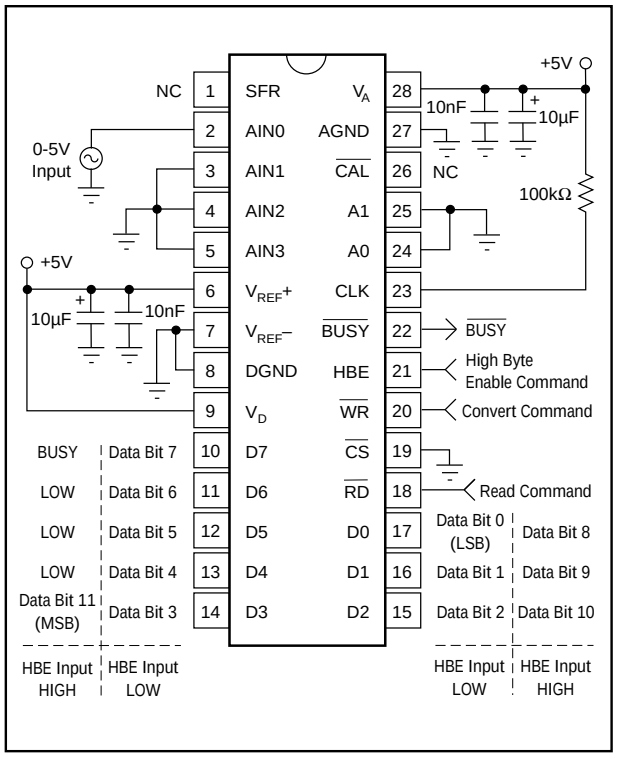


FIGURE 1. Basic Operation.

Figures 2 and 3 show the full conversion sequence and the timing to initiate a conversion.

CALIBRATION

A calibration cycle is initiated automatically upon power-up (or after a power failure). Calibration can also be initiated by the user at any time by the rising edge of a minimum 100ns-wide LOW pulse on the $\overline{CAL}$ pin (pin 26), or by setting D1 HIGH in the Special Function Register (see SFR section). A calibration command will initiate a calibration cycle, regardless of whether a conversion is in process. During a calibration cycle, convert commands are ignored.

Calibration takes 168 clock cycles, and a normal conversion (17 clock cycles) is added automatically. For maximum accuracy, the supplies and reference need to be stable during the calibration procedure. To ensure that supply voltages and reference voltages have settled and are stable, an internal timer provides a waiting period of 42,425 clock cycles between power-up/power-failure and the start of the calibration cycle.

READING DATA

Data from the ADC7802 is read in two 8-bit bytes, with the Low byte containing the 8 LSBs of data, and the High byte containing the 4 MSBs of data. The outputs are coded in straight binary (with 0V = 000 hex, 5V = FFF hex), and the data is presented in a right-justified format (with the LSB as the most right bit in the 16-bit word). Two read operations are required to transfer the High byte and Low byte, and the bytes are presented according to the input level on the High Byte Enable pin (HBE).

The bytes can be read in either order, depending on the status of the HBE input. If HBE changes while $\overline{CS}$ and $\overline{RD}$ are LOW, the output data will change to correspond to the HBE input. Figure 4 shows the timing for reading first the Low byte and then the High byte.

ADC7802 provides two modes for reading the conversion results. At power-up, the converter is set in the Transparent Mode.

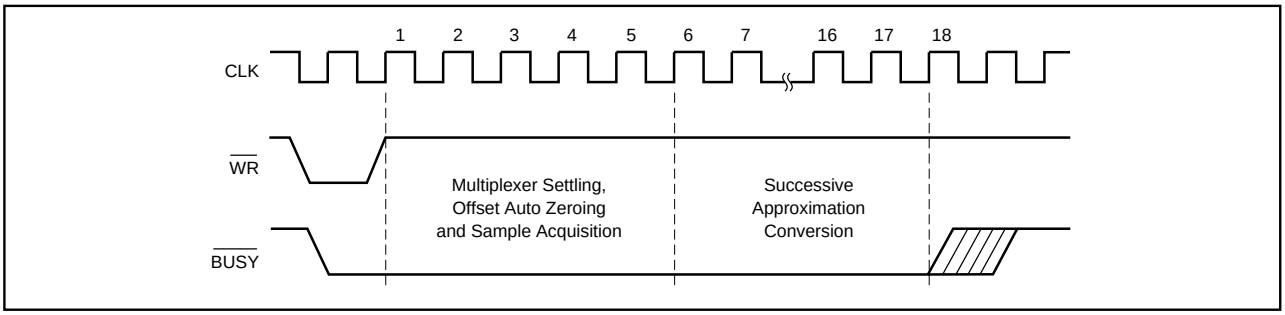


FIGURE 2. Converter Timing.

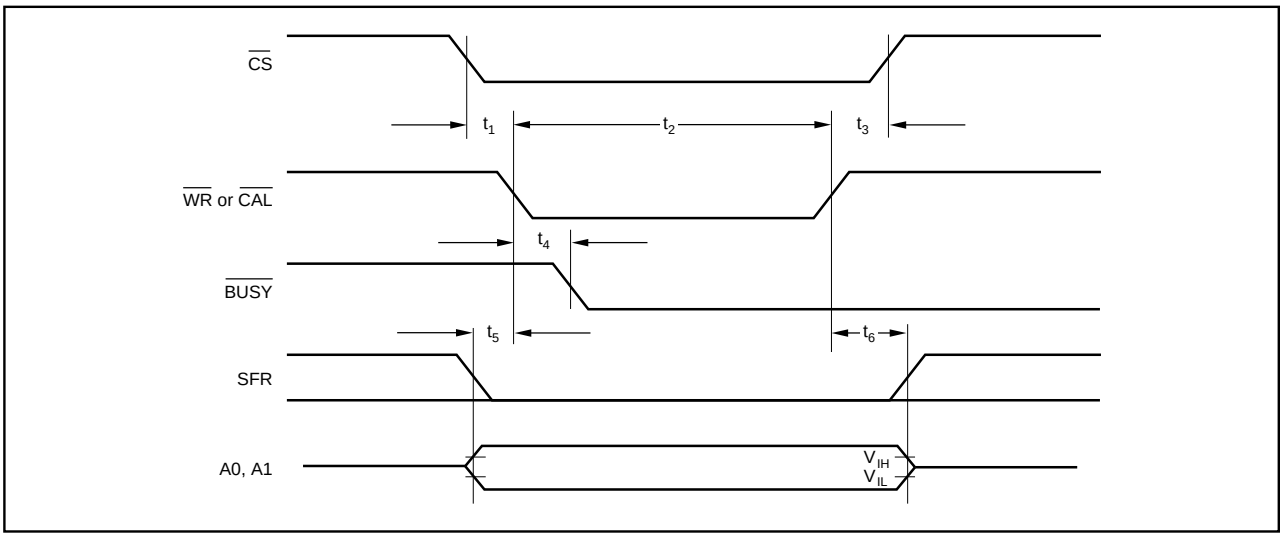


FIGURE 3. Write Cycle Timing (for initiating conversion or calibration).

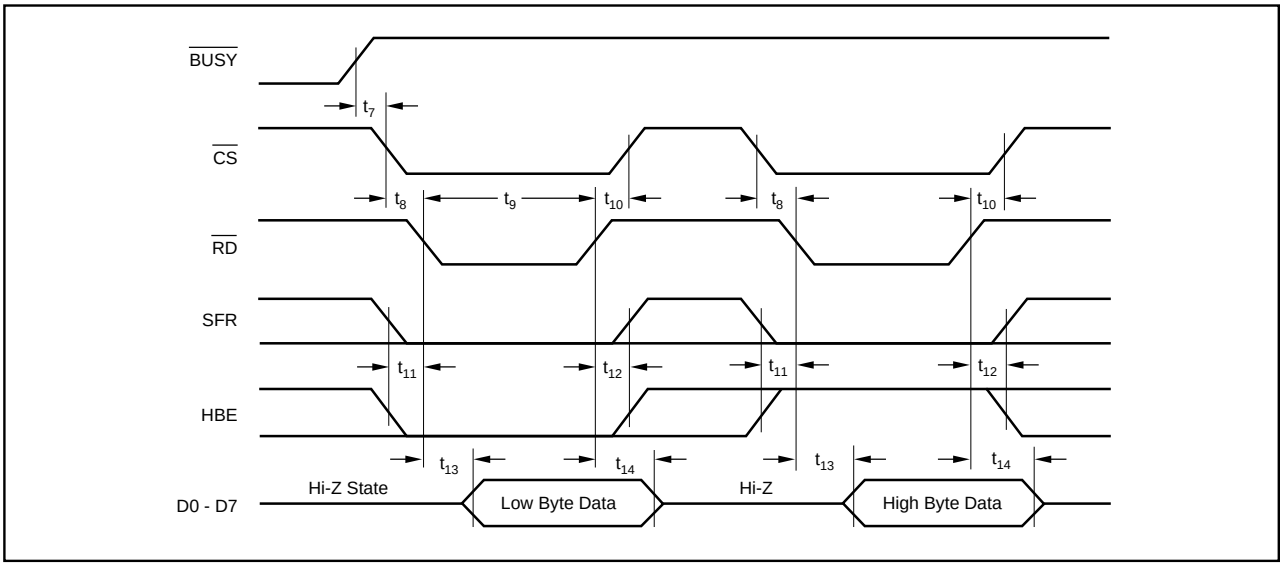


FIGURE 4. Read Cycle Timing.

TRANSPARENT MODE

This is the default mode for ADC7802. In this mode, the conversion decisions from the successive approximation register are latched into the output register as they are made. Thus, the High byte (the 4 MSBs) can be read after the end of the ninth clock cycle (five clock cycles for the mux settling, sample acquisition and auto-zeroing of the comparator, followed by the four clock cycles for the 4MSB decisions.) The complete 12-bit data is available after $\overline{BUSY}$ has gone HIGH, or the internal status flag goes LOW (D7 when HBE is HIGH).

LATCHED OUTPUT MODE

This mode is activated by writing a HIGH to D0 and LOWs to D1 to D7 in the Special Function Register with $\overline{CS}$ and $\overline{WR}$ LOW and SFR and HBE HIGH. (See the discussion of the Special Function Register below.)

In this mode, the data from a conversion is latched into the output buffers only after a conversion is complete, and remains there until the next conversion is completed. The conversion result is valid during the next conversion. This allows the data to be read even after a new conversion is started, for faster system throughput.

TIMING CONSIDERATIONS

Table I and Figures 3 through 8 show the digital timing of ADC7802 under the various operating modes. All of the critical parameters are guaranteed over the full –40°C to +85°C operating range for ease of system design.

SPECIAL FUNCTION REGISTER (SFR)

An internal register is available, either to determine additional data concerning the ADC7802, or to write additional instructions to the converter. Access to the Special Function Register is made by driving SFR HIGH.

SYMBOL	PARAMETER (1)	MIN	TYP	MAX	UNITS
t_1	$\overline{CS}$ to $\overline{WR}$ Setup Time (2)	0	0	0	ns
t_2	$\overline{WR}$ or $\overline{CAL}$ Pulse Width	100			ns
t_3	$\overline{CS}$ to $\overline{WR}$ Hold Time (2)	0	0	0	ns
t_4	$\overline{WR}$ to $\overline{BUSY}$ Propagation Delay	20	50	150	ns
t_5	A0, A1, HBE, SFR Valid to $\overline{WR}$ Setup Time	0			ns
t_6	A0, A1, HBE, SFR Valid to $\overline{WR}$ Hold Time	20			ns
t_7	$\overline{BUSY}$ to $\overline{CS}$ Setup Time	0			ns
t_8	$\overline{CS}$ to $\overline{RD}$ Setup Time (2)	0	0	0	ns
t_9	$\overline{RD}$ Pulse Width	100			ns
t_{10}	$\overline{CS}$ to $\overline{RD}$ Hold Time (2)	0	0	0	ns
t_{11}	HBE, SFR to $\overline{RD}$ Setup Time	50			ns
t_{12}	HBE, SFR to $\overline{RD}$ Hold Time	0			ns
t_{13}	$\overline{RD}$ to Valid Data (Bus Access Time) (3)		80	150	ns
t_{14}	$\overline{RD}$ to Hi-Z Delay (Bus Release Time) (3)		90	180	ns
t_{15}	$\overline{RD}$ to Hi-Z Delay For SFR (3)	20		60	ns
t_{16}	Data Valid to $\overline{WR}$ Setup Time	100			ns
t_{17}	Data Valid to $\overline{WR}$ Hold Time	20			ns

NOTES: (1) All input control signals are specified with $t_{RISE} = t_{FALL}$ = 20ns (10% to 90% of 5V) and timed from a voltage level of 1.6V. Data is timed from V_{IH}, V_{IL}, V_{OH} or V_{OL}. (2) The internal RD pulse is performed by a NOR wiring of $\overline{CS}$ and $\overline{RD}$. The internal $\overline{WR}$ pulse is performed by a NOR wiring of $\overline{CS}$ and $\overline{WR}$. (3) Figures 7 and 8 show the measurement circuits and pulse diagrams for testing transitions to and from Hi-Z states.

TABLE I. Timing Specifications (CLK = 1MHz external, T_A = –40°C to +85°C).

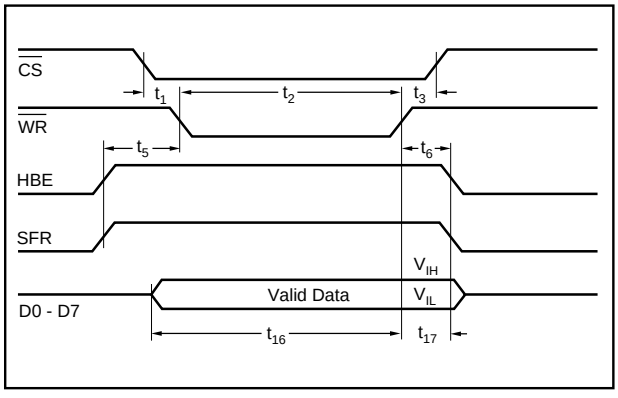


FIGURE 5. Writing to the SFR.

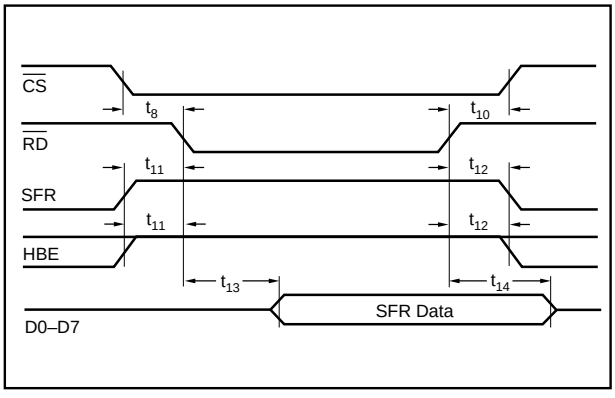


FIGURE 6. Reading the SFR.

Table II shows the data in the Special Function Register that will be transferred to the output bus by driving HBE HIGH (with SFR HIGH) and initiating a read cycle (driving $\overline{RD}$ and $\overline{CS}$ LOW with $\overline{WR}$ HIGH as shown in Figure 4.) The Power Fail flag in the SFR is set when the power supply falls below about 3V. The flag also means that a new calibration has been started, and any data written to the SFR has been lost. Thus, the ADC7802 will again be in the Transparent Mode. Writing a LOW to D5 in the SFR resets the Power Fail flag. The Cal Error flag in the SFR is set when an overflow occurs during calibration, which may happen in very noisy systems. It is reset by starting a calibration, and remains low after a calibration without an overflow is completed.

Writing a HIGH to D3 in the FSR puts the ADC7802 in the Power Down Mode. Power consumption is reduced to 50µW and D3 remains HIGH. To exit Power Down Mode, either write a LOW to D3 in the SFR, or initiate a calibration by sending a LOW to the $\overline{CAL}$ pin or writing a HIGH to D1. During Power Down Mode, a pulse on $\overline{CS}$ and $\overline{WR}$ will initiate a single conversion, then the ADC7802 will revert to power down.

Table III shows how instructions can be transferred to the Special Function Register by driving HBE HIGH (with SFR HIGH) and initiating a write cycle (driving $\overline{WR}$ and $\overline{CS}$ LOW with $\overline{RD}$ HIGH.) The timing is shown in Figure 3. Note that writing to the SFR also initiates a new conversion.

PIN	FUNCTION	DESCRIPTION
D0	Mode Status	If LOW, Transparent Mode enabled for data latches. If HIGH, Latched Output Mode enabled.
D1	CAL Flag	If HIGH, calibration cycle in progress.
D2		Reserved for factory use.
D3	Power Down Status	If HIGH, in Power Down Mode.
D4		Reserved for factory use.
D5	POWER FAIL Flag	If HIGH, a power supply failure has occurred. (Supply fell below 3V.)
D6	CAL ERROR Flag	If HIGH, an overflow occured during calibration.
D7	BUSY Flag	If HIGH, conversion or calibration in progress.
NOTE: These data are transferred to the bus when a read cycle is initiated with SFR and HBE HIGH. Reading the SFR with SFR HIGH and HBE LOW is reserved for factory use at this time, and will yield unpredictable data.		

TABLE II. Reading the Special Function Register.

CONTROL LINES

Table IV shows the functions of the various control lines on the ADC7802. The use of standard $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$ control signals simplifies use with most microprocessors. At the same time, flexibility is assured by availability of status information and control functions, both through the SFR and directly on pins.

	$\overline{CS}/\overline{WR}$	SFR/HBE	D0	D1	D3	D5	D7	D2/D4/D6
Enables Transparent Mode for Data Latches.	LOW	HIGH	LOW	X	LOW	X	LOW	LOW
Enables Latched Output Mode for Data Latches.	LOW	HIGH	HIGH	X	LOW	X	LOW	LOW
Initiates Calibration Cycle.	LOW	HIGH	X	HIGH	LOW	X	LOW	LOW
Resets Power Fail flag.	LOW	HIGH	X	X	LOW	LOW	LOW	LOW
Activates Power Down Mode	LOW	HIGH	X	X	HIGH	X	LOW	LOW
NOTES: (1) In Power Down Mode, a pulse on $\overline{CS}$ and $\overline{WR}$ will initiate a single conversion, then the ADC7802 will revert to power down. (2) X means it can be either HIGH or LOW without affecting this action. Writing HIGH to D2, D3, D4 or D6, or writing with SFR HIGH and HBE LOW, may result in unpredictable behavior. These modes are reserved for factory use at this time.								

TABLE III. Writing to the Special Function Register.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	SFR	HBE	$\overline{CAL}$	$\overline{BUSY}$	OPERATION
X	X	X	X	X	0↑1	X	Initiates calibration cycle.
X	X	X	X	X	X	0	Conversion or calibration in process. Inhibits new conversion from starting.
1	X	X	X	X	1	X	None. Outputs in Hi-Z State.
0	1	0↑1	0	X	1	1	Initiates conversion.
0	0	1	0	0	1	X	Low byte conversion results output on data bus.
0	0	1	0	1	1	X	High byte conversion results output on data bus.
0	1	0	1	1	1	1	Write to SFR and rising edge on $\overline{WR}$ initiates conversion.
0	0	1	1	1	1	X	Contents of SFR output on data bus.
0	1	0	1	0	1	X	Reserved for factory use.
0	0	1	1	0	1	X	Reserved for factory use. (Unpredictable data on data bus.)

TABLE IV. Control Line Functions.

INSTALLATION

INPUT BANDWIDTH

From the typical performance curves, it is clear that ADC7802 can accurately digitize signals up to 500Hz, but distortion will increase beyond this point. Input signals slewing faster than 8mV/µs can degrade accuracy. This is a result of the high-precision auto-zeroing circuit used during the acquisition phase. For applications requiring higher signal bandwidth, any good external sample/hold, like the SHC5320, can be used.

INPUT IMPEDANCE

ADC7802 has a very high input impedance (input bias current over temperature is 100nA max), and a low 50pF input capacitance. To ensure a conversion accurate to 12 bits, the analog source must be able to charge the 50pF and settle within the first five clock cycles after a conversion is initiated. During this time, the input is also very sensitive to noise at the analog input, since it could be injected into the capacitor array.

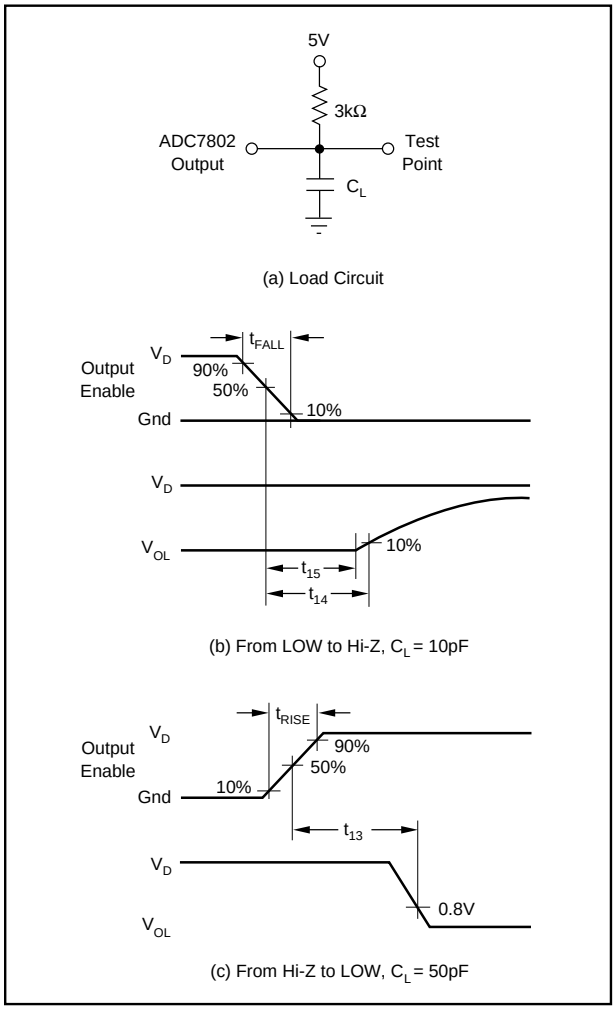


FIGURE 7. Measuring Active LOW to/from Hi-Z State.

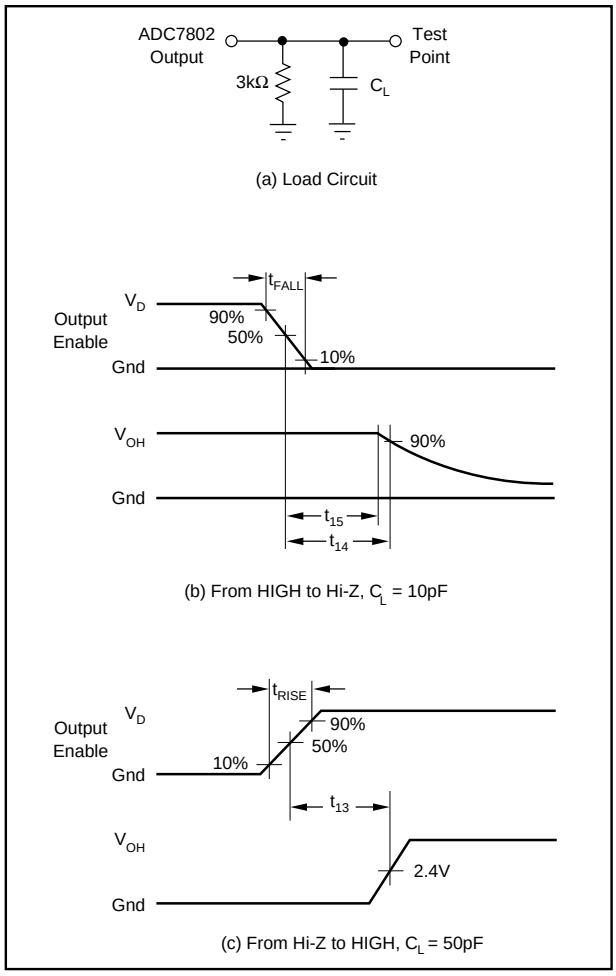


FIGURE 8. Measuring Active HIGH to/from Hi-Z State.

In many applications, a simple passive low-pass filter as shown in Figure 9a can be used to improve signal quality. In this case, the source impedance needs to be less than 5kΩ to keep the induced offset errors below 1/2LSB, and to meet the acquisition time of five clock cycles. The values in Figure 9a meet these requirements, and will maintain the full power bandwidth of the system. For higher source impedances, a buffer like the one in Figure 9b should be used.

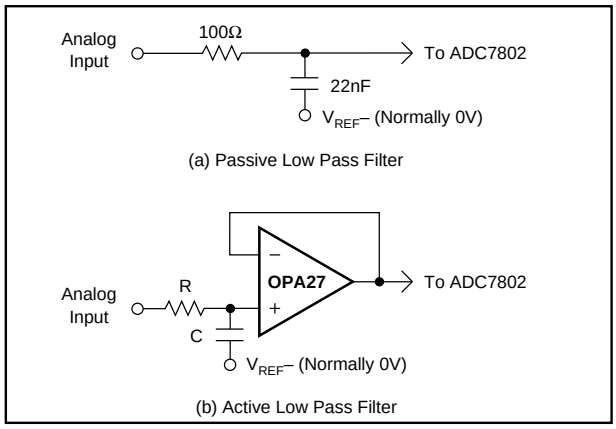


FIGURE 9. Input Signal Conditioning.

INPUT PROTECTION

The input signal range must not exceed $\pm V_{REF}$ or V_A by more than 0.3V.

The analog inputs are internally clamped to V_A. To prevent damage to the ADC7802, the current that can flow into the inputs must be limited to 20mA. One approach is to use an external resistor in series with the input filter resistor. For example, a 1kΩ input resistor allows an overvoltage to 20V without damage.

REFERENCE INPUTS

A 10µF tantalum capacitor is recommended between $V_{REF}+$ and $V_{REF}–$ to insure low source impedance. These capacitors should be located as close as possible to the ADC7802 to reduce dynamic errors, since the reference provides packets of current as the successive approximation steps are carried out.

$V_{REF}+$ must not exceed V_A. Although the accuracy is specified with $V_{REF}+ = 5V$ and $V_{REF}– = 0V$, the converter can function with $V_{REF}+$ as low as 2.5V and $V_{REF}–$ as high as 1V. As long as there is at least a 2.5V difference between $V_{REF}+$ and $V_{REF}–$, the absolute value of errors does not change significantly, so that accuracy will typically be within ±1LSB. (1/2LSB for a 5V span is 610µV, which is 1LSB for a 2.5V span.)

The power supply to the reference source needs to be considered during system design to prevent $V_{REF}+$ from exceeding (or overshooting) V_A, particularly at power-on. Also, after power-on, if the reference is not stable within 42,425 clock cycles, an additional calibration cycle may be needed.

POWER SUPPLIES

The digital and analog power supply lines to the ADC7802 should be bypassed with 10µF tantalum capacitors as close to the part as possible. Although ADC7802 has excellent power supply rejection, even for higher frequencies, linear regulated power supplies are recommended.

Care should be taken to insure that V_D does not come up before V_A, or permanent damage to the part may occur. Figure 10 shows a good supply approach, powering both V_A and V_D from a clean linear supply, with the 10Ω resistor between V_A and V_D insuring that V_D comes up after V_A. This is also a good method to further isolate the ADC7802 from digital supplies in a system with significant switching currents that could degrade the accuracy of conversions.

GROUNDING

To maximize accuracy of the ADC7802, the analog and digital grounds are not connected internally. These points should have very low impedance to avoid digital noise feeding back into the analog ground. The $V_{REF}–$ pin is used as the reference point for input signals, so it should be connected directly to AGND to reduce potential noise problems.

EXTERNAL CLOCK OPERATION

The circuitry required to drive the ADC7802 clock from an external source is shown in Figure 11a. The external clock must provide a 0.8V max for LOW and a 3.5V min for HIGH, with rise and fall times that do not exceed 200ns. The minimum pulse width of the external clock must be 200ns. Synchronizing the conversion clock to an external system clock is recommended in microprocessor applications to prevent beat-frequency problems.

Note that the electrical specification tables are based on using an external 2MHz clock. Typically, the specified accuracy is maintained for clock frequencies between 0.5 and 2.2MHz.

INTERNAL CLOCK OPERATION

Figure 11b shows how to use the internal clock generating circuitry. The clock frequency depends only on the value of the resistor, as shown in "Internal Clock Frequency vs R_{CLOCK}" in the Typical Performance Curves section.

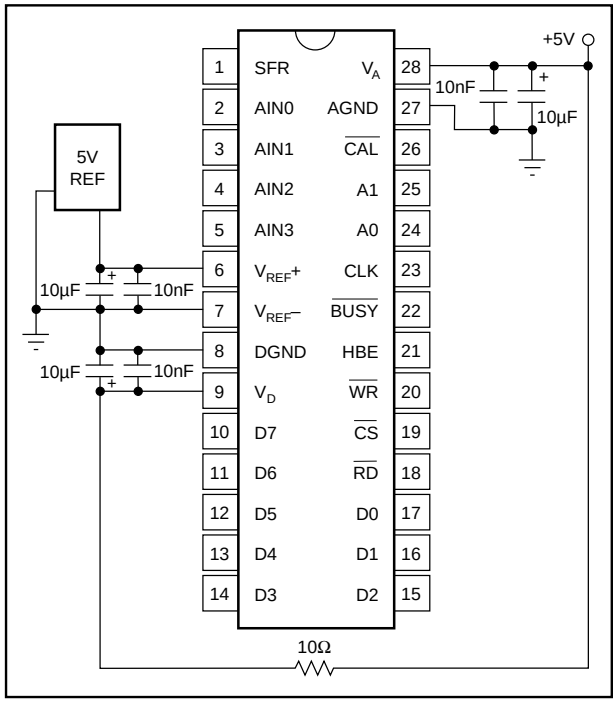


FIGURE 10. Power Supply and Reference Decoupling.

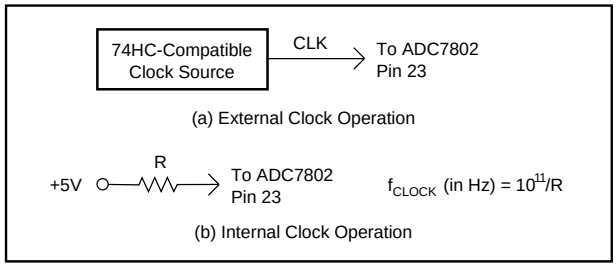


FIGURE 11. Internal Clock Operation.

The clock generator can operate between 100kHz and 2MHz. With R = 100kΩ, the clock frequency will nominally be 800kHz. The internal clock oscillators may vary by up to 20% from device to device, and will vary with temperature, as shown in the typical performance curves. Therefore, use of an external clock source is preferred in many applications where control of the conversion timing is critical, or where multiple converters need to be synchronized.

APPLICATIONS

BIPOLAR INPUT RANGES

Figure 12 shows a circuit to accurately and simply convert a bipolar ±5V input signal into a unipolar 0 to 5V signal for conversion by the ADC7802, using a precision, low-cost complete difference amplifier, INA105.

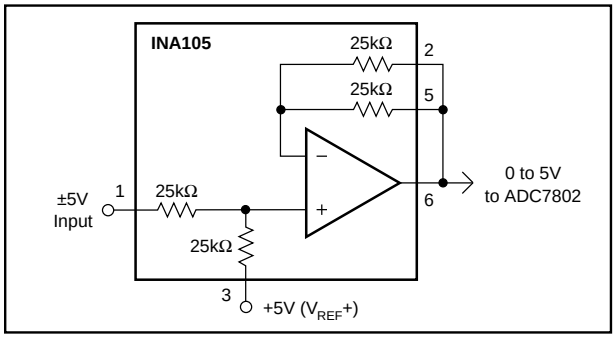


FIGURE 12. ±5V Input Range.

Figure 13 shows a circuit to convert a bipolar ±10V input signal into a unipolar 0 to 5V signal for conversion by the ADC7802. The precision of this circuit will depend on the matching and tracking of the three resistors used.

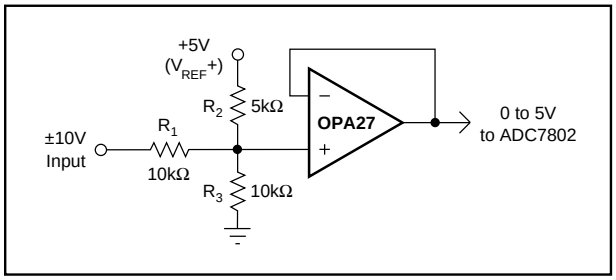


FIGURE 13. ±10V Input Range.

To trim this circuit for full 12-bit precision, R2 and R3 need to be adjustable over appropriate ranges. To trim, first have the ADC7802 converting continually and apply +9.9927V (+10V – 1.5LSB) at the input. Adjust R3 until the ADC7802 output toggles between the codes FFE hex and FFF hex. This makes R3 extremely close to R1. Then, apply –9.9976V (–10V + 0.5LSB) at the input, and adjust R2 until the ADC7802 output toggles between 000 hex and 001 hex. At each trim point, the current through the third resistor will be almost zero, so that one trim iteration will be enough in most cases. More iterations may be required if the op amp selected has large offset voltage or bias currents, or if the +5V reference is not precise.

This circuit can also be used to adjust gain and offset errors due to the components preceding the ADC7802, to match the performance of the self-calibration provided by the converter.

INTERFACING TO MOTOROLA MICROPROCESSORS

Figure 14 shows a typical interface to Motorola microprocessors, while Figure 15 shows how the result can be placed in register D0.

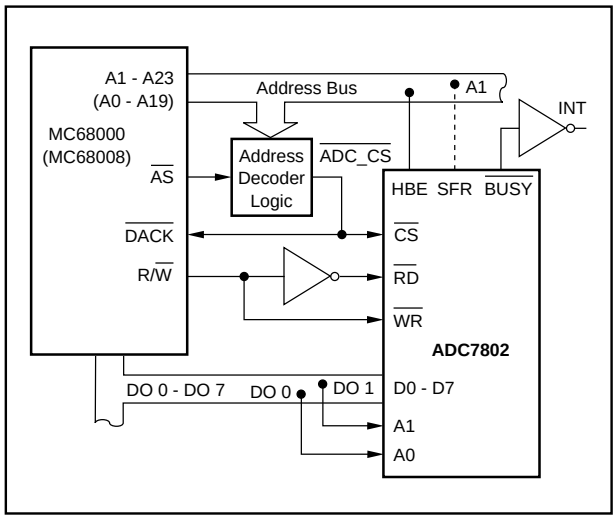


FIGURE 14. Interface to Motorola Microprocessors.

Conversion is initiated by a write instruction decoded by the address decoder logic, with the lower two bits of the address bus selecting an ADC input channel, as follows:

MOVE.W D0, ADC-ADDRESS

The result of the conversion is read from the data bus by a read instruction to ADC-ADDRESS as follows:

MOVEP.W $000 (ADC-ADDRESS), D0

This puts the 12-bit conversion result in the DO register, as shown in Figure 15. The address decoder must pull down $\overline{\text{ADC\_CS}}$ at ADC-ADDRESS to access the Low byte and ADC-ADDRESS +2 to access the High byte.

INTERFACING TO INTEL MICROPROCESSORS

Figure 16 shows a typical interface to Intel.

A conversion is initiated by a write instruction to address $\overline{\text{ADC\_CS}}$. Data pins DO0 and DO1 select the analog input channel. The $\overline{\text{BUSY}}$ signal can be used to generate a microprocessor interrupt (INT) when the conversion is completed.

A read instruction from the $\overline{\text{ADC\_CS}}$ address fetches the Low byte, and a read instruction from the $\overline{\text{ADC\_CS}}$ address +2 fetches the High byte.

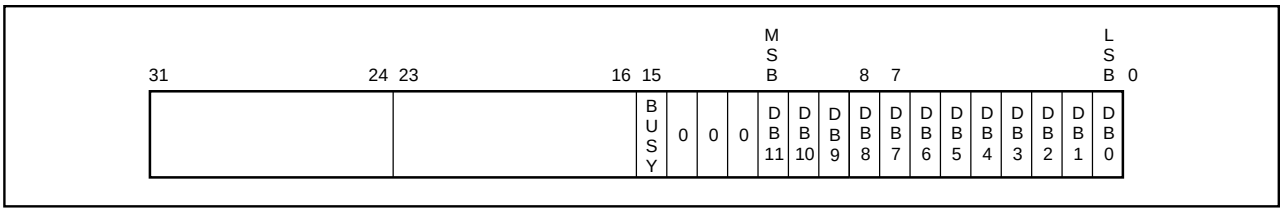


FIGURE 15. Conversion Results in Motorola Register D0.

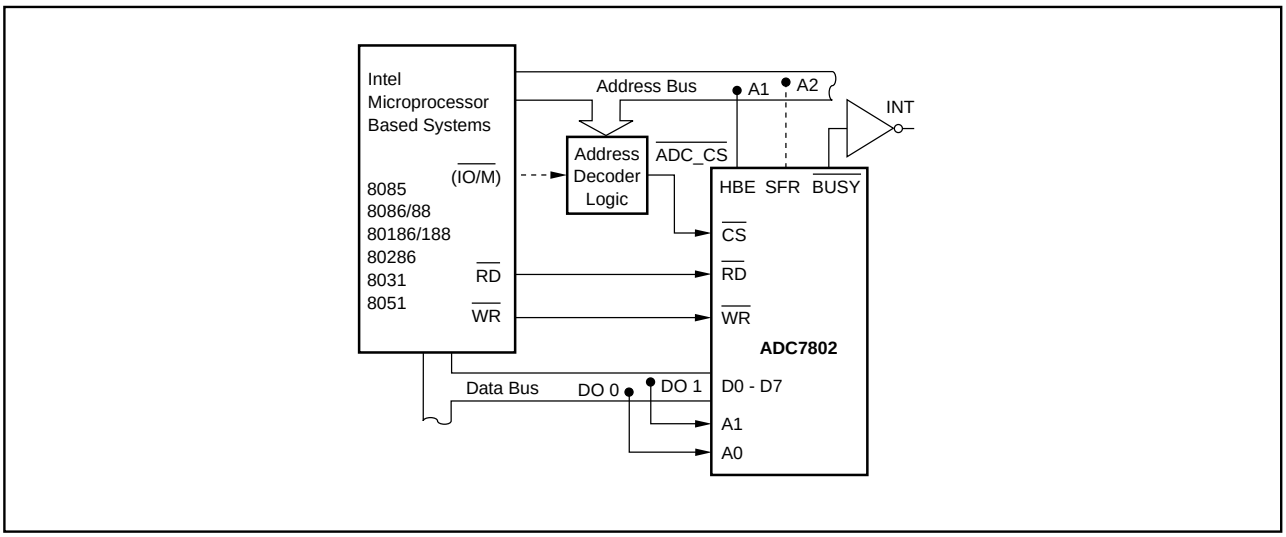


FIGURE 16. Interface to Intel Microprocessors.